REMARKS

The present Amendment amends claims 1, 3, 5, 7, 8, 13, 15 and 20-22, cancels claim 4, leaves claims 6, 9-12, 14 and 19 unchanged, and adds new claims 24-35. Therefore, the present application has pending claims 1 and 3, 5-14 and 16-35.

In the Office Action the Examiner alleges that the specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicants have reviewed the specification. However, Applicants were unable to locate any such minor errors. Therefore, Applicants respectfully request the Examiner to identify any errors the Examiner may be aware of so that the specification can be immediately amended to expedite prosecution of the present application.

Claims 1, 21 and 22 stand objected to due to informalities noted by the Examiner in paragraphs 3 and 4 of the Office Action. Amendments were made to claims 1, 21 and 22 to correct the informalities noted by the Examiner. Therefore, this objection is overcome and should be withdrawn.

Claims 3 and 15 stand rejected under 35 USC §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regards as their invention. Various amendments were made throughout claims 3 and 15 to overcome the 35 USC §112, second paragraph rejection. Therefore, this rejection is overcome and should be withdrawn. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

Applicants acknowledge the Examiner's indication in paragraph 28 of the Office Action that claims 7-9 would be allowable if rewritten in independent

form including all the limitations of the base claim and any intervening claims. Amendments were made to claims 7-9 to place them in independent form including all the limitations of the base claim and any intervening claims. Therefore, claims 7-9 are allowable as indicated by the Examiner.

Claims 1, 3-5, 10, 12, 13, 16, 18 and 20-23 stand rejected under 35 USC §102(e) as being anticipated by Glasco (U.S. Patent Application Publication No. 2003/0225909); claims 6 and 17 stand rejected under 35 USC §103(a) as being unpatentable over Glasco in view of Adams (U.S. Patent No. 6,124,878); and claims 11, 14 and 19 stand rejected under 35 USC §103(a) as being unpatentable over Glasco and further in view of Casamatta (EP No. 0 908 825). As indicated above, claim 4 was canceled. Therefore, the above 35 USC §102(e) rejection with respect to claim 4 is rendered moot. With respect to the remaining claims, these rejections are traversed for the following reasons. Applicants submit that the features of the present invention as now more clearly recited in claims 1 and 3-6 and 10-14 and 16-23 are not taught or suggested by Glasco, Adams or Casamatta whether taken individually or in combination with each other as suggested by the Examiner. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw these rejections.

Amendments were made to claims 1, 13, 20 and 21 so as to more clearly describe features of the present invention not taught or suggested by any of the references of record whether taken individually or in combination with each other. Particularly, amendments were made to these claims to more clearly recite that the present invention is directed to an information

processing device, a memory controlled device and an information processing method which processes information used in a plurality of processors.

According to the present invention, the information processing device includes one or more first processors that have a plurality of first local memories, one or more second processors which performs one of directly writing write information into a target first local memory that a target first processor selected from among the first processors, has and directly reading information from the target first local memory and an address map memory means for storing a first address map in which the first local memory addresses for each of the one or more first processors are recorded.

Further, according to the present invention each of the one or more second processors performs one of acquiring the first local memory address of the target first processor from the first address map, writing the write information into the acquired first local memory address and reading the read information from the acquired first local memory address.

Still further, according to the present invention, a relay device is provided that receives the write information from the one or more second processors and transfers the write information to the target first processor. According to the present invention the relay device includes a relay memory and wherein when transferring the write information, the relay device selectively performs an operation of the transfer after the write information temporarily stored in the relay memory or an operation of the transfer without storing the write information in the relay memory. These features of the present invention regarding the relay device were originally recited in claims 4 and 15. Thus, the subject matter of these claims was inserted into

independent claims 1, 13, 20 and 21. It should be noted and emphasized that these features are presently recited in claims 22 and 23 also.

The above described features of the present invention are not taught or suggested by any of the references of record whether taken individually or in combination with each other.

The above described features of the present invention now more clearly recited in the claims are not taught or suggested by Glasco.

Glasco teaches, for example, a multi-processor computer system in which address mapping routing and transaction identification mechanisms are provided which enable the interconnection of a plurality of multi-processor clusters. Particularly, Glasco provides an interconnection controller for use in a computer system having a plurality of processor clusters and a global address space associated therewith. Each cluster includes a plurality of local nodes an instance of the interconnection controller interconnected by a local point-to-point architecture. As per Glasco, each cluster has a local address space associated therewith corresponding to a first portion of the global address space. Further, as per Glasco, the interconnection controller includes circuitry which is operable to map locally generated address information to others of the clusters in the global address space and remotely generated address information to the local nodes in the local address space.

However, at no point is there any teaching or suggestion in Glasco of the above described features of the present invention now more clearly recited in the claims wherein a relay device is provided which receives the write information from the one or more second processors and transfers the write information to the target first processor. Further, there is no teaching or

suggestion in Glasco that the relay device includes a relay memory and that when transferring the write information, the relay device selectively performs an operation of the transfer after the write information temporarily stored in the relay memory or an operation of the transfer without storing the write information in the relay memory as in the present invention.

In the Office Action the Examiner alleges that Glasco teaches such features. However, Glasco teaches, for example, in Fig. 8 thereof that information is always entered into a buffer such as, for example, in Step 808 of Fig. 8. However, there is no teaching or suggestion in Glasco that selective information can be selectively entered into the buffer or not as in the present invention. Thus, at no point is there any teaching or suggestion in Glasco of any element corresponding to the relay device as recited in the claims.

Further, there is no teaching or suggestion in Glasco that each of the one or more second processors performed one of the acquiring the local memory address of the target first processor from the first address map, writing the write information into the acquired first local memory address and reading the read information from the acquired first local memory address as in the present invention. Such features are clearly not taught or suggested by Glasco.

Thus, Glasco fails to teach or suggest a relay device which receives the write information from the one or more second processors and transfers the write information to the target first processor wherein the relay device comprises a relay memory and wherein when transferring the write information, the relay device selectively performs an operation of the transfer after the write information temporarily stored in the relay memory, or an

operation of the transfer without storing the write information in the relay memory as recited in the claims.

Further, Glasco fails to teach or suggest address map memory means for storing a first address map in which the first local memory addresses for each of the one or more first processors are recorded, wherein each of the one or more second processors performs at least one of acquiring the first local memory address of the target first processor from the first address map, writing the write information into the acquired first local memory address, and reading the read information from the acquired first local memory address as recited in the claims.

Therefore, Glasco fails to teach or suggest the features of the present invention as now more clearly recited in the claims. Accordingly, reconsideration and withdrawal of the 35 USC §102(e) rejection of claims 1, 3-5, 10, 12, 13, 16, 18 and 20-23 as being anticipated by Glasco is respectfully requested.

The above described deficiencies of Glasco are not supplied by Adams or Casamatta whether taken individually or in combination with each other.

Adams is merely relied upon for an alleged teaching that if the amount information accumulated in the write information storage region exceeds a first threshold value, a notification of exceeding the first threshold value, which indicates that this threshold value has been exceed is transmitted to the second device and that the second device that is the notification of exceeding the first threshold value reduces the frequency with which write information is issued or the amount of the information that is issued to the target local memory or the target first processor. Applicants do not agree with the

Examiner's assessment. However, even if the above described teaching alleged by the Examiner to exist in Adams is true, Adams does not teach or suggest the above described features now more clearly recited in the claims regarding the address map memory means and the relay device.

Thus, combining the teachings of Glasco with the teachings of Adams in the manner suggested by the Examiner in the Office Action still fails to teach or suggest the features of the present invention as now more clearly recited in the claims.

The above noted deficiencies of Glasco and Adams are also evident in Casamatta. Accordingly, combining the teachings of Glasco with one or more of Adams and Casamatta still fails to teach or suggest the features of the present invention as now more clearly recited in the claims.

Therefore, the 35 USC §103(a) rejection of claims 6 and 17 as being unpatentable over Glasco in view of Adams and the 35 USC §103(a) rejection of claims 11, 14 and 19 as being unpatentable over Glasco in view of Casamatta is respectfully requested.

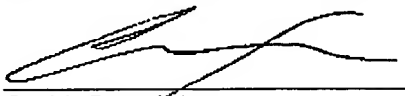
The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references utilized in the rejection of claims 1-23.

In view of the foregoing amendments and remarks, applicants submit that claims 1 and 3, 5-14 and 16-35 are in condition for allowance. Accordingly, early allowance of claims 1 and 3, 5-14 and 16-35 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C., Deposit Account No. 50-1417 (1309.43464X00).

Respectfully submitted,

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.



Carl I. Brundidge
Registration No. 29,621

CIB/jdc
(703) 684-1120